Question: 01

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | Processor | Hexadecimal Code  | Behavioral RTL  |
| JPL R5, [26] | Falcon - A | 851A | R[5]>0(PC=PC+26) |
| STS R7, R2 (100) | Falcon - E | 2F400064 | M[R[2]+100]←R[7] |
| STACC R4, 36 | Modified EAGLE | BC24 | M[R[4]+(8a36)©36]←ACC |
| DIV R2 | EAGLE | 82 | R[0]←R[0]/R[2]R[2]←R[0]%R[2] |
| SHIFTL R5, R2, 7 | FALCON - A | 6547 | R[5]←r[2]<8..2>©(7a0) |

**Question NO: 02**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Instruction | Contents stored in Destination Operand | Data Bus | Address Bus | Calculation Steps |
| LDACC B |  55CE | 55CE | 3320 | destination: ACC←content of B which is M[B+1]©M[B]data bus::M[B+1]©M[B]Address bus: address of B |
| SUB R1 | 55B9 |  |  | destination: ACC←content of ACC-r1No read & write for data and address bus. |
| LDACC C | 2015 | 2015 | AB0E | destination: ACC←content of CData bus:M[C+1]©M[C]Address bus:Address of C |
| ADD R2 | 45E0 |  |  | destination: ACC←content of ACC+r2No read & write for data and address bus. |
| STACC A | 45E0 | 45E0 | AB10 | destination: A←content of ACC data bus: content of ACCAddress bus: address of A |